

A NEW LOAD-PULL CHARACTERIZATION METHOD  
FOR MICROWAVE POWER TRANSISTORS

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Abstract

A novel method for microwave power transistor load-pull characterization is presented. The method provides an equivalent load-pull measurement technique without using an output impedance tuner. In this method, both input and output ports of a test transistor are simultaneously driven by external signals at the same specified frequency. Results of its application to a medium-power GaAs FET are given.

Introduction

In estimations and applications of microwave power transistors, including field-effect transistors, large-signal characterization is an essential procedure. S-parameter characterization, to describe large-signal characteristics of power transistors, is generally inadequate, except in some specific cases<sup>2</sup>. Load-pull characterization is a recommended approach, which was successfully applied to transistor power amplifier designs.<sup>3, 4</sup> The usual load-pull measurement is made, using an ultraprecision calibrated impedance tuner. However, at high frequencies, such as C- and X-bands, it is fairly difficult to realize a reliable impedance tuner.

The purpose of this paper is to present a novel method for microwave power transistor load-pull characterization. This method provides an equivalent load-pull measurement technique without using an output impedance tuner. In this method, both input and output ports of a test transistor are simultaneously driven by external signals at a specified frequency. This procedure realizes equivalent variation of the transistor load on the whole impedance plane. Results of its application to a medium-power GaAs FET are presented. This method is especially expected to be most applicable at high frequency ranges where reliable impedance tuners cannot be easily obtained.

Transistor Large-Signal Characterization

Assuming the transistor operation of short-circuited harmonics, if the input and output ac terminal voltages are defined to be

$$V_i = \tilde{V}_i e^{j\omega t} \text{ and } V_0 = \tilde{V}_0 e^{j(\omega t + \theta)}, \quad (1)$$

respectively, the admittances, looking into the transistor input and output, can be described as

$$Y_1(\omega, \tilde{V}_i, \tilde{V}_0, \theta) \text{ and } Y_2(\omega, \tilde{V}_i, \tilde{V}_0, \theta), \quad (2)$$

respectively. These admittances, as a function of  $\omega$ ,  $\tilde{V}_i$ ,  $\tilde{V}_0$  and  $\theta$ , characterize the large-signal operating state of the transistor under a specified dc bias condition. They can be measured by simultaneously driving the input and output of the transistor by the external signals at the same specified frequency. The proposed equivalent load-pull method is fundamentally based on this understanding.

Principle of Equivalent Load-Pull Method

A basic network for the principle explanation of the equivalent load-pull method is shown in Fig. 1. There is a fixed tuning network at the transistor input. The transistor output, which is represented by reference plane A, is connected to impedance measure-

ment equipment, such as a network analyzer. The input and output of the transistor are driven simultaneously by external signals at the same specified frequency. An external signal into the transistor output varies an ac terminal voltage and that equivalently corresponds to the load-variation of the transistor output. In Fig. 1,  $V_2$  and  $V_3$  are the incident and reflected voltage waves, respectively, at output reference plane A. Incident and reflected powers at the transistor output are expressed by

$$P_2 = \frac{1}{2} Y_0 \tilde{V}_2^2 \text{ and } P_3 = \frac{1}{2} Y_0 \tilde{V}_3^2, \quad (3)$$

respectively, where  $\tilde{V}_2$  and  $\tilde{V}_3$  are the magnitudes of  $V_2$  and  $V_3$ , respectively, and  $Y_0$  is the characteristic admittance of the transmission line. When a given signal is delivered to the transistor input, the ac output terminal voltage  $V_0$  is given by

$$V_0 = V_2 + V_3 = \frac{2Y_0}{Y_0 + Y_2} \cdot V_2 \quad (4)$$

where  $Y_2$  is the dynamic admittance looking into the transistor output. Then, the equivalent admittance and reflection-coefficient, looking toward the output load, are given by

$$Y_L = -Y_2 \quad (5)$$
$$T_L = \frac{V_2}{V_3} = \frac{Y_0 - Y_L}{Y_0 + Y_L},$$

respectively. The transistor power output is obtained by

$$P_{out} = P_3 - P_2 = \frac{1}{2} G_L \tilde{V}_0^2 \quad (6)$$

where  $Y_L = G_L + jB_L$ . Therefore, under a given signal level  $P_{in}$ , delivered to the transistor input, the ac terminal voltage of the transistor output varies according to incident signal  $V_2$  delivered into the output. This corresponds to the equivalent transistor load variation.

Measurement Techniques

The experimental equipment arrangement for the equivalent load-pull measurement is shown in Fig. 2. A high level signal, provided by the TWT, is divided into two signals. One drives the transistor input, through the tuning network. The other signal drives the transistor output through the network analyzer reflection unit and the low-pass filter, whose VSWR at the test frequency is sufficiently low. The filter is not used where insignificant harmonics are excited. The signal level delivered to the transistor input is set at a specified level. Power level and phase of the signal into the transistor output are controlled using the variable attenuator and phase shifter, respective-

ly. Equivalent load admittance  $Y_L = -Y_2$  or equivalent load reflection-coefficient  $\Gamma_L$  is directly measured by making the reflected signal  $V_3$  the reference signal for the network analyzer system. Incident and reflected signal power levels  $P_2$  and  $P_3$  are also monitored. Transistor output power  $P_{out}$  is obtained from the power expression (6) or by measuring the voltage difference between DVM outputs of two power meters used to monitor  $P_2$  and  $P_3$  levels. The equivalent load impedance was plotted by using an X-Y recorder.

#### Application to GaAs Power FET

The proposed equivalent load-pull method was applied to determining the characteristics of a source-grounded GaAs MESFET, which was developed for medium-power applications in our laboratory<sup>5</sup>. The FET chip is mounted on a test carrier, which has  $50\Omega$  microstrip input and output ports formed on 1 mm-thick alumina substrates. The output reference plane for the transistor is placed on the beginning of the drain-output stripline, where drain electrodes are wire-bonded. Measurements were made at 6 GHz. Transistor input drive level was fixed at 95.5 mW. The FET input tuner network was tuned to match the transistor input. Fig. 3 shows loci of the load impedance at constant incident power levels into the FET output port, with the phase of the incident signal into the FET output as a parameter. Fig. 4 shows the load impedance contours for constant power outputs.

#### Conclusion

A novel method for accomplishing load-pull characterization of microwave power transistors has been presented. This method, which provides a load-pull measurement technique without using an output impedance tuner, may be called an equivalent load-pull measurement method. In this method, both input and output of a test transistor are simultaneously driven by external signals at the same specified frequency. This procedure enables equivalent variation of the transistor load-impedance on the whole impedance plane. Load-pull characteristics of a microwave medium-power GaAs FET have been measured with the proposed method. This particular technique is expected to be most applicable at high frequency ranges where reliable impedance tuners cannot be obtained.

#### Acknowledgment

The author would like to thank T. Ogawa for his technical assistance and M. Takeuchi, A. Higashisaka, R. Yamamoto and F. Hasegawa for supplying the GaAs FETs. He would also like to thank K. Ayaki for his encouragement and guidance.

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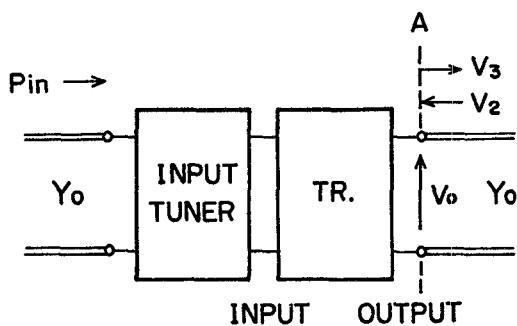


Fig.1 Basic network for equivalent load-pull method principle explanation.

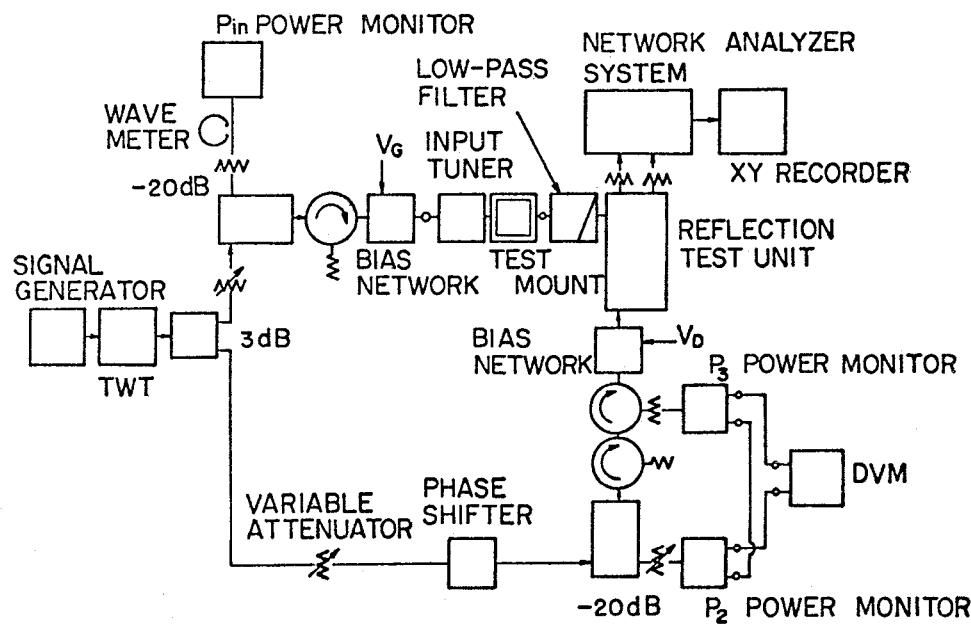


Fig.2 Setup for equivalent load-pull measurement.

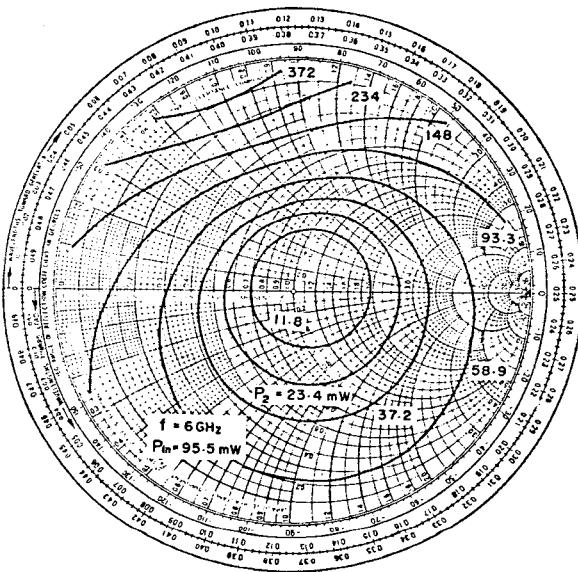


Fig.3 Loci of load impedance at 6 GHz for a GaAs FET at several incident power levels into FET output with incident signal phase into FET output as a parameter.

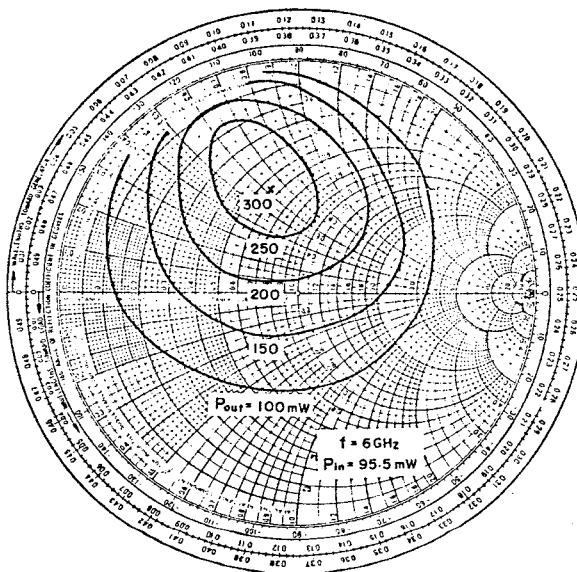


Fig.4 FET load impedance contours at 6 GHz for constant power outputs at 95.5 mW input power level.